What is claimed is

1. A semiconductor device comprising:

a semiconductor substrate;

a silicon oxide layer formed over a surface of said semiconductor substrate;

a gate electrode formed over a first portion of said silicon oxide layer; and

a side wall structure formed over a second portion of said silicon oxide layer and adjacent said gate electrode,

wherein a thickness of said second portion of said silicon oxide layer is greater than a thickness of said first portion of said silicon oxide layer.

2. A semiconductor device as claimed in claim.1,

wherein the thickness of said second portion of said silicon oxide layer is at least twice the thickness of said first portion of said silicon oxide layer.

3. A semiconductor device as claimed in claim.1,

wherein the thickness of said second portion of said silicon oxide layer is at least 50% greater than the thickness of said first portion of said silicon oxide layer.

4.. A semiconductor device comprising:

a semiconductor substrate;

a gate oxide layer formed over said semiconductor substrate;

a gate electrode formed over a first portion of said gate oxide layer;

a side wall structure formed adjacent said gate electrode; and

a diffusion deterrent layer formed between said side wall structure and said semiconductor substrate;

wherein a thickness of said diffusion deterrent layer is greater than a thickness of said first portion of said gate oxide layer.

5. A method for manufacturing a semiconductor device, comprising:

forming a gate oxide layer on a surface of a semiconductor substrate;

forming a gate electrode and over a first portion of said gate oxide layer;

forming a cap layer over said gate electrode;

expanding a thickness of a second portion of said gate oxide layer other than said first portion located under said gate electrode;

forming a side wall structure on said second portion of said gate oxide layer and adjacent said gate electrode;

forming intermediate insulating layer over said cap layer and said side wall structure; and

forming a contact hole in said intermediate insulating layer using a Self Aligned Contact process.

6. A method for manufacturing a semiconductor device as claimed in claim. 5, wherein the thickness of said second portion of said silicon oxide layer is at least twice the thickness of said first portion of said silicon oxide layer.

7. A method for manufacturing a semiconductor device as claimed in claim. 5, wherein the thickness of said second portion of said silicon oxide layer is at least 50% greater than the thickness of said first portion of said silicon oxide layer.

8. A method for manufacturing a semiconductor device as claimed in claim. 5, wherein the thickness of said second portion of said gate oxide layer is expanded using CVD.

9. A method for manufacturing a semiconductor device as claimed in

claim. 6, wherein the thickness of said second portion of said gate oxide layer is expanded using CVD.

10. A method for manufacturing a semiconductor device as claimed in claim. 7, wherein the thickness of said second portion of said gate oxide layer is expanded using CVD.

11. A method for manufacturing a semiconductor device as claimed in claim.5, wherein the thickness of said second portion of said gate oxide layer is expanded using thermal oxidation.

12. A method for manufacturing a semiconductor device as claimed in claim.6, wherein the thickness of said second portion of said gate oxide layer is expanded using thermal oxidation.

13. A method for manufacturing a semiconductor device as claimed in claim.7, wherein the thickness of said second portion of said gate oxide layer is expanded using thermal oxidation.

14. A method for manufacturing a semiconductor device, comprising:

forming a gate oxide layer on a surface of a semiconductor substrate;

forming a gate electrode over a first portion of said gate oxide layer;

forming a cap layer over said gate electrode;

forming a side wall structure over a second portion of said gate oxide layer and adjacent said gate electrode;

expanding the thickness of said second portion of said gate oxide layer located under said side wall structure using thermal oxidation;

forming intermediate insulating layer over said cap layer and said side wall structure;

forming a contact hole in said intermediate insulating layer using a Self

Aligned Contact process.

15. A method for manufacturing a semiconductor device as claimed in claim.14, wherein said expanding the thickness of said second portion of said gate oxide layer is performed after formation of said intermediate insulating layer.

16. A method for manufacturing a semiconductor device, comprising:

forming a gate oxide layer on the surface of a semiconductor substrate;

forming a gate electrode over a first portion of said gate oxide layer;

forming a cap layer over said gate electrode;

forming a side wall structure on a second portion of said gate oxide layer and adjacent said gate electrode;

forming intermediate insulating layer over said cap layer and said side wall structure; and

forming a contact hole in said intermediate insulating layer using a Self Aligned Contact process;

wherein the side wall structure is formed by CVD at the temperature exceeding 850 ℃

17. A method for manufacturing a semiconductor device, comprising:

forming a gate oxide layer on the surface of a semiconductor substrate;

forming a gate electrode over a first portion of said gate oxide layer;

forming a cap layer over said gate electrode;

forming a first portion of side wall structure over a second portion of said gate oxide layer and adjacent said gate electrode;

forming a second portion of side wall structure over a second portion of said gate oxide layer and adjacent said gate electrode;

forming intermediate insulating layer over said cap layer and said side wall structure; and

forming a contact hole in said intermediate insulating layer using a Self Aligned Contact process;

wherein said first portion of side wall structure is formed by CVD at the temperature exceeding 850 ℃

18. A method for manufacturing a semiconductor device, comprising:

forming a gate oxide layer on a surface of a semiconductor substrate;

forming a gate electrode over a first portion of said gate oxide layer;

forming a cap layer over said gate electrode;

conducting a first ion implantation step to form a the shallow portion of an LDD region using said cap layer as a mask;

conducting a second ion implantation to form a deep portion of the LDD region using said cap layer as a mask;

forming a side wall structure on a second portion of said gate oxide layer and adjacent said gate electrode;

forming intermediate insulating layer on said semiconductor substrate; and

forming a contact hole in said intermediate insulating layer using a Self Aligned Contact process.